The current release of the Feng Shui standard cell placement tool is Version 1.5. It features a traditional bicriteria-based approach, using the Mhmetis multilevel partitioning library. Cut sequences are determined using a dynamic programming based technique (see DAC2001 paper "Improved Cut Sequences for Bicriteria-Based Placement"). To improve initial partitions, we use an iterative deletion approach (see GLSVLSI2001 paper "Global Objectives for Standard Cell Placement"). Source code and executable versions of Feng Shui Standard Cell Placer version 1.5 are available on the research group web site.

Recent enhancements:
- Improved GUI, allowing zoom, pan, and individual cell selection.
- LEF/DEF, GSRC Bookshelf, and TimberWolf file support.
- Improved GUI, allowing zoom, pan, and individual cell selection.
- LEF/DEF, GSRC Bookshelf, and TimberWolf file support.

The Feng Shui tools utilize a library of interconnect structure and delay analysis routines. Included in this set are an efficient Steiner tree heuristic based on prior work by Borah, Owen and Teen. The lengths are comparable to those of the 1-Steiner algorithm, but with low algorithmic complexity.

The Steiner heuristic has been extended to handle non-Manhattan routing architectures (see GLSVLSI2000 "Manhattan or non-Manhattan? A Study of Alternative Routing Architectures") and to consider routing congestion and via cost (see GLSVLSI2001 "Prefered Direction Steiner Trees" and an upcoming TCAD version).

Current work focuses on fast and accurate delay estimation for use in performance driven placement and routing. Our current method obtains estimates within a few percent of SPICE, but with compute times that are comparable to Dimos Delay. Our method uses a distributed delay model, and can consider inductance and complex drive circuit models.

The Feng Shui suite includes an interactive tool that allows shifting of pin positions to observe dynamic changes in route topology and delay.

Recent enhancements:
- Combined preferred direction and non-Manhattan topology integration of inductance into the delay estimation.
- Further speed and memory improvement for delay estimation.

Upcoming release:
- First public release planned for later this summer.

Students involved:
- Patrika Agarwal, Arvind Vidyarthi, Ameya Agnihotri, Mehmet Can YILDIZ.
- Support: IBM and SRC.

The area router uses a gridless model that simplifies integration of variable width routing and spacing constraints. The core algorithms center around combinatorial optimization, rather than more traditional rip-up and reroute. Consideration of all routes simultaneously allows for substantial reductions in crossover capacitance as much as 70% for some benchmarks, using a relatively simple coupling model.

The algorithmic approach has been integrated into one commercial routing tool and is being used for fast pre-router of complex designs.

Current work focuses on integration of a traditional maze-routing based approach to be used in conjunction with the the combinatorial methods. The maze router uses an underlying trapezoid tile database (to support both Manhattan and non-Manhattan designs), similar to methods described by Marlite.

Computational geometry methods are being integrated into the tool, to improve run time and increase the size of problems that can be handled.

Recent enhancements:
- Improved graphical user interface, including interactive three-dimensional viewing.
- Support for crosstalk reduction.

Upcoming release:
- Planned release at the end of summer.

Consideration of switching windows.
- Support for optimized interconnect and shielding of noise sensitive wires.
- Routling in multiple voltage environments.
- Support for RET and phase-INH lithography.

Students Involved:
- Raja Hadsell, Ameya Agnihotri.
- Support: NSF.